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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/164,898	10/01/1998	JAMES AKIYAMA	42390.P3373	7208

7590 08/24/2004

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EXAMINER

VITAL, PIERRE M

ART UNIT	PAPER NUMBER
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2188

DATE MAILED: 08/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/164,898

Applicant(s)

AKIYAMA, JAMES

Examiner

Pierre M. Vital

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 18 June 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 19-37 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 19-37 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 08 September 2000 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed June 18, 2004 in response to PTO Office Action mailed May 12, 2004. The Applicant's remarks and amendments to the claims and/or the specification were considered with the results that follow.
2. Claims 19-37 have been presented for examination in this application. In response to the last Office Action, claim 36 has been amended. No claims have been canceled or added. As a result, claims 19-37 are now pending in this application.

Response to Arguments

3. Applicant's arguments filed June 18, 2004 have been fully considered but they are not persuasive. As to the remarks, Applicant asserted that:

The prior art of record does not teach or suggest "the data written to and read from the first and second disk drives is interleaved so that even sectors are accessed on the first disk drive and odd sectors are accessed on the second disk drive" and that "alternating even-numbered and odd-numbered blocks of sectors between drives" is not equivalent to "alternating only even-numbered and odd-numbered sectors between drives".

Examiner respectfully traverses applicant's arguments for the following reasons.

Examiner agrees with applicant that "blocks contain a plurality of sectors" and that blocks could contain both even and odd numbered sectors. However, Examiner would also like to point out that odd-numbered blocks could contain odd-numbered sectors and even-numbered blocks could contain even-numbered sectors if the sectors are not sequentially organized in the blocks.

Turning to the prior art, Klein discloses that when data is being transferred, even-numbered blocks of sectors are accessed on the first disk drive and odd-numbered blocks of sectors are accessed on the second disk drive as detailed in column 4, lines 35-43. Klein further discloses that "other algorithms such as sector-by-sector interleaving and track-by-track interleaving, etc. may be used consistent with his invention" (see column 6, lines 26-29). As such, Examiner would like to emphasize that the sector-by-sector interleaving disclosed by Klein is the same as the even and numbered sector interleaving claimed by Applicant, since Klein could also access even sectors on the first drive and odd sectors on the second drive by implementing a sector-by-sector interleaving algorithm disclosed.

Thus, it can be clearly seen that although Klein discloses even and odd numbered blocks interleaving, Klein also discloses even and odd sector interleaving by providing for the implementation of even and odd numbered sectors interleaving algorithm in his invention.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 19-21, 25-30 and 35-36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein (US6,567,864) and Jones et al. (US5,619,723) and Thompson et al (US6,341,342) and further in view of Klein et al (US5,671,439).

As per claims 19, 25, 28 and 35, Klein ('864) discloses a system comprising: a Basic Input/Output System (BIOS) [*ROM BIOS 70*; Fig. 1; col. 3, lines 52-59]; a system bus coupled to said BIOS [*ROM BIOS 70 coupled to I/O bus 62*; Fig. 1; col. 3, lines 52-54]; an integrated drive electronics (IDE) interface coupled to said system bus that communicates directly with said BIOS via said system bus [*BIOS 70 cause the microprocessor 50 to initiate a DMA transfer from each of the IDE devices 66-68*; Fig. 1; col. 4, 50-53].

However, Klein ('864) fails to specifically teach a striping controller coupled to said IDE interface; a first disk drive including first IDE electronics, said striping controller coupled to said first IDE electronics; and a second disk drive including second IDE electronics, said striping controller coupled to said second IDE electronics, said first and second IDE electronics each having data separator electronics, data formatting electronics and head positioning electronics; wherein the data written to and read from

the first and second disk drives is interleaved so that even sectors are accessed on the first disk drive and odd sectors are accessed on the second disk drive as recited in the claims.

Thompson discloses a striping controller coupled to an IDE interface [Fig. 1B, *PCI-IDE adapter card 158*]; a first disk drive including first IDE electronics, a striping controller coupled to said first IDE electronics; and a second disk drive including second IDE electronics, said striping controller coupled to said second IDE electronics [*controller on same card as disk drives 124, 126; controller 118 coupled to drives 124, 126; Fig. 1B, col. 6, lines 35-55*] for reducing the number of queued commands that must be serviced by the array controller during disk drive operation (col. 3, lines 6-8, 24-25).

Jones discloses first and said second disk drives each having data separator electronics, data formatting electronics and head positioning electronics for increasing information transfer speed by allowing parallel read/writes by the disk drives [col.14, lines 30-55; col. 6, lines 7-9].

Klein ('439) discloses the data written to and read from the first and second disk drives is interleaved so that even sectors are accessed on the first disk drive and odd sectors are accessed on the second disk drive to transfer data at least twice the maximum sustainable data transfer rate of each drive [*means for alternately transfer even-numbered blocks between the on-board memory of the first drive and odd-numbered blocks between the on-board memory of the first drive; col. 4, lines 35-43; other algorithms such as sector-by-sector may be used; col. 6, lines 26-39*].

It would have been obvious to one of ordinary skill in the art, having the teachings of Klein ('864) and Thompson and Jones and Klein ('439) before him at the time the invention was made, to modify the system taught by Klein ('864) to include a striping controller coupled to an IDE interface and IDE electronics of Thompson because it was well known to provide faster controller operation by reducing the number of queued commands that must be serviced by the array controller during disk drive operation as taught by Thompson and include the disk drives electronics of Jones because it was well known to increase information transfer speed by allowing parallel read/writes by the disk drives as taught by Jones and include alternately reading even-numbered sectors from the first drive and odd-numbered sectors from the second drive because it was well known to provide increase sustainable data rate by transferring data at least twice the maximum sustainable data transfer rate of each drive as taught by Klein ('439).

As per claims 20, 27, 29 and 36, the combination of Klein ('864) and Jones and Thompson and Klein ('439) discloses the claimed invention as detailed above in the previous paragraphs. However, the combination of Klein ('864) and Thompson and Klein ('439) does not specifically teach a striping controller causing data to be written to and read from the first and second drives in an interleaved form and substantially in parallel as recited in the claims.

Jones discloses a striping controller causing data to be written to and read from the first and second drives substantially in parallel [col. 16, lines 32-35] to increase

information transfer speed by allowing parallel read/writes by the disk drives (col. 6, lines 7-9).

It would have been obvious to one of ordinary skill in the art, having the teachings of the combination of Klein ('864) and Jones and Thompson and Klein ('439) before him at the time the invention was made, to modify the system of Klein ('864) and Thompson and Klein ('439) to include a striping controller causing data to be written to and read from the first and second drives substantially in parallel because it was well known to increase information transfer speed by allowing parallel read/writes by the disk drives as taught by Jones.

As per claims 21 and 30, Thompson discloses data being transmitted between the system bus and the first and second disk drives is subdivided into a plurality of sequential blocks [col. 1, lines 43-54].

As per claim 26, Thompson discloses receiving an IDE request at a striping controller [col. 7, lines 4-25].

6. Claims 22, 31 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein (US6,567,864) and Jones et al. (US5,619,723) and Thompson et al (US6,341,342) and Klein et al (US5,671,439) and further in view of Anderson (US5,905,910).

As per claims 22 and 31, the combination of Thompson and Jones and Klein teach the claimed invention as detailed above in the previous paragraphs. However, neither Klein ('864) nor Thompson nor Jones nor Klein ('439) specifically teach the first disk drive is accessed for every other block of data and the second disk drive is accessed for the remaining blocks; and a control logic receives a system request intended for a single physical drive from the system bus as recited in the claims.

Anderson teaches a first disk drive is accessed for every other block of data and a second disk drive is accessed for the remaining blocks [col.11, lines 35-50; col.12, lines 3-23] to reduce disk access time and increase the efficiency of the system by allowing both disk drives to respond to commands that overlap in time (col. 12, lines 20-23).

It would have been obvious to one of ordinary skill in the art, having the teachings of Klein ('864) and Thompson and Jones and Klein ('439) and Anderson before him at the time the invention was made, to modify the system taught by Klein ('864) and Thompson and Jones and Klein ('439) to include the first disk drive is accessed for every other block of data and the second disk drive is accessed for the remaining blocks because it was well known to reduce disk access time and increase

the efficiency of the system by allowing both disk drives to respond to commands that overlap in time as taught by Anderson.

As per claim 34, the combination of Klein ('864) and Thompson and Jones and Klein ('439) discloses the claimed invention as detailed above in the previous paragraphs. However, neither Klein ('864) nor Thompson nor Jones nor Klein ('439) specifically discloses a control logic receiving a system request intended for a single physical drive from the system bus as recited in the claim.

Anderson discloses a control logic receiving a system request intended for a single physical drive from the system bus [col. 7, lines 60-63] to reduce disk access time and increase the efficiency of the system by allowing both disk drives to respond to commands that overlap in time (col. 12, lines 20-23).

It would have been obvious to one of ordinary skill in the art, having the teachings of Klein ('864) and Thompson and Jones and Klein ('439) and Anderson before him at the time the invention was made, to modify the system taught by Klein ('864) and Thompson and Jones and Klein ('439) to include a control logic that receives a system request intended for a single physical drive from the system bus because it was well known to reduce disk access time and increase the efficiency of the system by allowing both disk drives to respond to commands that overlap in time as taught by Anderson.

7. Claims 23, 24, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Klein (US6,567,864) and Jones et al. (US5,619,723) and Thompson et al (US6,341,342) and Klein et al (US5,671,439) and further in view of Jenkins (US4,047,157).

As per claims 23, 24, 32 and 33, the combination of Klein ('864) and Thompson and Jones and Klein ('439) discloses the claimed invention as detailed above in the previous paragraphs. However, neither Klein ('864) nor Thompson nor Jones nor Klein ('439) specifically discloses that the system request includes a sector bit string, a head bit string, a track bit string and a driver bit; and mapping bits of the system request to a first system request data structure to be supplied to the first disk drive and a second system request data structure to be supplied to the second disk drive as recited in the claims.

Jenkins teaches a controller for use in a data processing system wherein in the track/sector register 146 Track Address and Sector Address bit positions identify, respectively, the track and sector on a disk to be involved in a transfer; in a fixed-head unit, the Track Address bits identify a specific head [col. 20, lines 38-42]; a Write signal, produced in response to the function bits, enables drivers 297 to load data onto the data set 101 [col. 26, lines 26-28]; and mapping bits of the system request to a first system request data structure to be supplied to the first disk drive and a second system request data structure to be supplied to the second disk drive [col. 20, lines 38-65] to improve processing speeds and memory access times by providing the system identification

information for the physical location on the drive from which the data file will be read or written (col. 2, lines 28-30).

It would have been obvious to one of ordinary skill in the art, having the teachings of Klein ('864) and Thompson and Jones and Klein ('439) and Jenkins before him at the time the invention was made, to modify the system taught by Klein ('864) and Thompson and Jones and Klein ('439) to include sector bit string, head bit string, track bit string and driver bit in the system request and mapping bits of the system request to a first system request data structure to be supplied to the first disk drive and a second system request data structure to be supplied to the second disk drive because it was well known to improve processing speeds and memory access times by providing the system identification information for the physical location on the drive from which the data file will be read or written as taught by Jenkins.

8. Claim 37 is rejected under 35 U.S.C. 103(a) as being unpatentable over Klein (US6,567,864) and Jones et al. (US5,619,723) and Thompson et al (US6,341,342) and Klein et al (US5,671,439) and further in view of Mizuno et al (US5,608,891).

As per claim 37, the combination of Klein ('864) and Thompson and Jones and Klein ('439) teach the claimed invention as detailed above in the previous paragraphs. However, neither Klein ('864) nor Thompson nor Jones nor Klein ('439) specifically teach a first FIFO memory coupled to an XOR gate and driven by a signal from the XOR

gate to access a first storage device and a second FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a second storage device as recited in the claim.

Mizuno discloses a first FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a first storage device and a second FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a second storage device [col. 17, lines 8-28] to improve system performance by reducing the time required for temporarily storing write data in memory and then exclusive Oring the data to find redundant data (col. 18, lines 46-53).

It would have been obvious to one of ordinary skill in the art, having the teachings of Klein ('864) and Thompson and Jones and Klein ('439) and Mizuno before him at the time the invention was made, to modify the system taught by Klein ('864) and Thompson and Jones and Klein ('439) to include a first FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a first storage device and a second FIFO memory coupled to an XOR gate and driven by a signal from the XOR gate to access a second storage device because it was well known to improve system performance by reducing the time required for temporarily storing write data in memory and then exclusive Oring the data to find redundant data as taught by Mizuno.

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

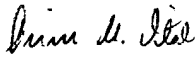
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pierre M. Vital whose telephone number is (703) 306-5839. The examiner can normally be reached on Mon-Fri, 8:30 am - 6:00 pm, alternate Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

August 9, 2004


Pierre M. Vital
Examiner
Art Unit 2188